REMARKS

Claims 19-32 are pending in the current application. In an office action dated March 19, 2009 ("Office Action"), the Examiner rejected claims 19, 24-26, and 30-32 under 35 U.S.C. § 102(e) as being anticipated by Lucas, U.S. Patent Application No. 2004/0010746 ("Lucas"). Applicants and Applicants' representative wish to thank the Examiner for the conditional allowance of claims 20-23 and 27-29, but defer rewriting these claims in independent form until the Examiner has had an opportunity to consider the following traversal of the 35 U.S.C. § 102(e) rejections of claims 19, 24-26, and 30-32.

Please consider claim 19:

> 19. An apparatus for denoising an input noisy signal, the apparatus comprising:
> one or more memories; and
> a controller that
> receives the noisy signal *z* that includes a number of sequentially ordered symbols, each symbol having a position,
> stores the noisy signal *z* in the one or more memories,
> receives a signal *r*, output from a preliminary denoising system that operates on the received noisy signal *z*, that includes a number of sequentially ordered symbols, each symbol having a position,
> stores the signal *r* in the one or more memories, and
> produces an output signal *z'* by replacing a symbol within each of a number of different subsequences that occur in the noisy signal *z* with a corresponding replacement symbol that the controller computes to provide a minimal estimated signal degradation.

The Examiner reads the controller, claimed in the second element of claim 19, onto Lucas' address generator (301 in Figure 3 of Lucas). Please note that the currently claimed controller carries out the four operations that include: (1) storing the noisy signal *z* in the one or more memories; (2) receiving a signal *r*, output from a preliminary denoising system that operates on the received noisy signal *z*, that includes a number of sequentially ordered symbols, each symbol having a position; (3) storing the signal *r* in the one or more memories; and (4) producing an output signal *z'* by replacing a symbol

within each of a number of different subsequences that occur in the noisy signal *z* with a corresponding replacement symbol that the controller computes to provide a minimal estimated signal degradation. Please note that Figure 3 of Lucas "is a more detailed block diagram of an exemplary embodiment of the rank value filter of FIG. 2." The rank value filter ("RVF") is shown as block 209 in Figure 2 of Lucas. Please note also that Figure 2 of Lucas "is a more detailed block diagram illustrating a portion of an exemplary configuration of the RX processor of FIG. 1 interfaced to a portion of the MAC interface that includes a MAC buffer." The RX processor is shown, in Figure 1 of Lucas, as a component 121 of a baseband processor 107. As discussed by Lucas, in paragraph [0034], Lucas' address generator controls addressing of a series of memories within the RVF component of an RX-processor component of a baseband processor. As discussed in paragraph [0029] of Lucas, the RVF "ranks the currently stored SQ metrics from highest to lowest quality." The RVF does not receive a noisy signal, does not store a noisy signal, does not receive a signal output from a output from a preliminary denoising system, and does not produce an output signal by replacing a symbol within each of a number of different subsequences that occur in the noisy signal *z* with a corresponding replacement symbol that the controller computes to provide a minimal estimated signal degradation. Nothing in paragraph [0034] or in any other paragraph of Lucas teaches, mentions, or even suggests that Lucas' address generator 301 is anything other than an address generator. It produces a replace symbol number (RSN) signal that is shown in Figure 2 to be output to the CRC logic block 211. This signal (identifies which of the old set of SYM2 and SQ metric values is being replaced. This has nothing at all to do with producing "an output signal *z'* by replacing a symbol within each of a number of different subsequences that occur in the noisy signal *z* with a corresponding replacement symbol that the controller computes to provide a minimal estimated signal degradation." As is clearly shown in Figure 2 of Lucas, output of a signal is produced by the control & logic output block 215. As discussed in paragraph [0032], it is the control & logic output block that produces an output signal in which symbols of an input signal are selectively replaced. The Examiner is incorrect in attempting to map the currently claimed controller onto Lucas' address generator.

Lucas is unrelated to the apparatus for denoising an input noisy signal to which claim 19 is directed. Lucas' forward-error correction system is based on cyclic redundancy code ("CRC") error checking. A CRC number is computed from the contents of a packet by a well-known CRC-number-generation algorithm, in this technique, and appended to the packet prior to transmission. Upon reception, the receiver recomputers the CRC number and compares the recomputed CRC number with the CRC number in the packet. When the transmitted CRC number matches the recomputed CRC number, the packet is deemed to have been transmitted without error. Otherwise, erroneous transmission has occurred. Depending on the length of the CRC number, one or a few erroneous bits may be identified and corrected. However, for errors that comprise more than a few erroneously transmitted bits, the receiver generally requests that the packet be resent by the transmitter.

Lucas seeks to provide a higher level of error correction by carrying out replacement of certain symbols in an erroneous packet, recomputing the CRC number, and then determining whether the recomputed CRC number matches the transmitted CRC number. When symbol replacement produces a matching CRC number, the symbol replacement is taken as the proper correction of errors, and the packet, with symbol replacement, is determined to be equivalent to the originally transmitted packet. This is discussed, in overview, in paragraphs [0004-0007] of Lucas. Details are provided from paragraph [0016] on, in the specification.

Clearly, Lucas is completely unrelated to the currently claimed apparatus, and similarly claimed method of independent claim 26. Again, please consider the following portions of claim 19:

> receives the noisy signal *z* that includes a number of sequentially ordered symbols, each symbol having a position,
>
> stores the noisy signal *z* in the one or more memories,
>
> receives a signal *r*, output from a preliminary denoising system that operates on the received noisy signal *z*, that includes a number of sequentially ordered symbols, each symbol having a position,
>
> stores the signal *r* in the one or more memories, and
>
> produces an output signal *z'* by replacing a symbol within each of a number of different subsequences that occur in the noisy signal *z* with a corresponding replacement symbol that the

controller computes to provide a minimal estimated signal degradation.

The apparatus to which claim 19 is directed receives a noisy signal *z* as well a denoised signal *r* produced by a preliminary denoising system, and stores them both in memory. Lucas does not teach, mention, or suggest preliminary denoising of a noisy signal. The apparatus to which claim 19 is directed uses both the noisy signal z and the preliminary denoised signal r to produce an output signal *z'* by replacing a symbol within each of a number of different subsequences that occur in the noisy signal *z* with a corresponding replacement symbol that the controller computes to provide a minimal estimated signal degradation. Lucas does not teach, mention, or suggest anything related to minimizing estimated signal degradation. Lucas simply carries out a single error-correction pass by choosing symbol replacements that result in generation of a CRC that matches the transmitted CRC. This has nothing to do with minimizing an estimated signal degradation. Lucas does not carry out a preliminary denoising step. Because Lucas is unrelated to the denoising apparatus and method of independent claims 19 and 26, Lucas cannot possibly anticipate these claims, or any claims that depend from them.

In Applicants' representative's opinion, all of the claims remaining in the current application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

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